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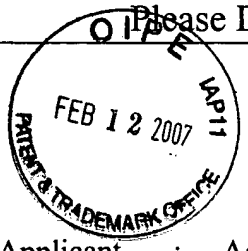

TRANSMITTAL LETTER
APPEAL BRIEF

Applicant	:	Aggarwal et al.
App. No	:	10/665,693
Filed	:	September 17, 2003
For	:	SYSTEM FOR THE IMPROVED HANDLING OF WAFERS WITHIN A PROCESS TOOL
Examiner	:	Adams, Gregory W.
Art Unit	:	3652

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

February 8, 2007
(Date)

Tina Chen, Reg. No. 44,606

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith in triplicate for filing in the above-identified application are the following enclosures:

(X) Appeal Brief in 16 pages.

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FEE CALCULATION				
FEE TYPE		**FEE CODE**	**CALCULATION**	**TOTAL**
Appeal Brief	*41.20(b)(2)*	1402 ($500)		$500
1 Month Extension	*1.17(a)(1)*	1251 ($120)		$0
2 Month Extension	*1.17(a)(2)*	1252 ($450)		$0
3 Month Extension	*1.17(a)(3)*	1253 ($1,020)		$0
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Docket No.	:	ASMEX.358DV1	**Customer No.: 20,995**
Application No.	:	10/665,693	
Filing Date	:	September 17, 2003	

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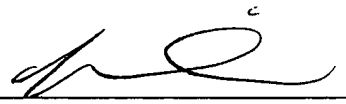
Dated: February 8, 2007



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Aggarwal et al.
Appl. No.	:	10/665,693
Filed	:	September 17, 2003
For	:	SYSTEM FOR THE IMPROVED HANDLING OF WAFERS WITHIN A PROCESS TOOL
Examiner	:	Adams, Gregory W.
Group Art Unit	:	3652

ON APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES
APPELLANT'S BRIEF

Mail Stop Appeal Brief -- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief relates to an appeal to the Board of Patent Appeals and Interferences of the final rejection set forth in a final Office Action mailed September 8, 2006 in the above-captioned application.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of this application, ASM America, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

The present application was originally filed with Claims 1-23, which are all currently pending in the present application and have been finally rejected in the Office Action mailed September 8, 2006, which final rejection was affirmed by an Advisory Action mailed November

13, 2006. Accordingly, Claims 1-23 are the subject of this appeal. These claims are attached hereto in the Claims Appendix.

IV. STATUS OF AMENDMENTS

The claims before the Board appear as they were finally rejected. No amendments to the claims have been filed subsequent to the final rejection. As noted above, these pending claims are attached hereto in the Claims Appendix.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention, as recited by the pending claims, relates generally to semiconductor fabrication, and more particularly to improved wafer handling systems.

Semiconductor substrates typically arrive at the input of a process tool and must be transported from the input into the process tool and among internal stations or chambers of the process tool. Process tools typically have wafer handling systems to transfer substrates. It is desirable to isolate the substrates from contamination, or at least minimize contamination of the substrates and the possibility of cross-contamination of the chambers of the process tool. Wafer handling systems may include standardized front opening unified pods (FOUPs) and loadlock chambers for minimizing substrate contamination. *See* Specification at paragraphs [0003]-[0005].

The present invention, as recited in the pending claims, provides a semiconductor process tool 5 having a FOUP 10 located on a front end interface (FEI) loading platform 12. The FOUP 10 is removably docked with a docking port 14 of the process tool 5. *See* Specification at paragraph [0035] and Figure 1. According to one embodiment of the invention, the docking port 14 is on the outside surface of a substrate handling chamber 22. *See id.*

The invention, in one embodiment, comprises a robot arm 24 in the chamber 22, which is configured to access a buffer station 30. *See* Specification at paragraphs [0035]-[0036] and Figure 1. The buffer station 30 is separated from the chamber 22 by buffer station doors 13. *See* Specification at paragraph [0036]. The buffer station 30 has a rack 38 with multiple shelves for holding multiple substrates, and can be purged with an internal environment that is separate from the substrate handling chamber 22 after the buffer station doors 13 are closed to separate the buffer station 30 from the substrate handling chamber 22 to minimize contamination. *See* Specification at paragraphs [0040] and [0043]. A loadlock chamber 40 is also joined to the

substrate handling chamber 22 and can be accessed by the robot arm 22. *See* Specification at paragraph [0038] and Figure 1.

Within a short time of docking the FOUP 10 with the docking port 14, the robot arm 24 transfers each wafer 20 from a cassette rack 16 in the FOUP 10 to the buffer station rack 38 in the buffer station 30. This transfer of wafers 30 from the FOUP 10 to the buffer station rack 38 may be immediate upon docking of the FOUP 10 with the docking port 14 on the outside of the substrate handling chamber 22. After completion of the transfer of wafers 20 to the buffer station rack 38, the buffer station doors 13 are closed to separate the buffer station 30 from the chamber 22, and the buffer station 30 is purged. *See* Specification at paragraph [0043] and Figures 3A and 3B. Purging the buffer station 30 creates an inert environment in which to store the substrates while waiting for processing. The inert environment in the purged buffer station 30 minimizes contamination of the substrates while they are stored and waiting for processing. *See* Specification at paragraph [0056].

The robot arm 24 then unloads the wafers 20 from the buffer station rack 38 and transfers them to a loadlock rack 46 in the loadlock chamber 40, as needed for processing. *See* Specification at paragraph [0044]. The robot arm 24 can cycle between the buffer station 30 and the loadlock chamber 40 until all wafers are processed. *See id.*

The present invention provides a semiconductor process tool 5 that allows multiple wafers 20 in a FOUP 10 to be quickly transported upon entry at a front docking port 14 to a purgeable buffer station 30 for storage. The buffer station 30 can be purged to have an inert environment, which is less contaminated than a clean room. The wafers are stored in the inert environment of the buffer station 30 until they are ready for processing and transferred to the loadlock chamber 40. *See* Specification at paragraph [0011]. Such an arrangement minimizes contamination of the wafers.

The appealed claims reflect the disclosed invention. Each of the pending claims recites a front docking port located on an outside surface of a substrate handling chamber and a purgeable buffer station adjacent the substrate handling chamber. For example, independent Claims 1 and 10 both recite, *inter alia*, a front docking port located on an outside surface of the first substrate handling chamber; a robot arm located in the first substrate handling chamber; a loadlock chamber joined to the first substrate handling chamber; and a buffer station adjacent the first substrate handling chamber and separate from the loadlock chamber, and the buffer station being purged with an inert internal environment separate from the first substrate handling chamber.

Independent Claim 14 recites, *inter alia*, a substrate handling chamber; a front docking port located on an outside surface of the substrate handling chamber, the port being capable of mating with a cassette; and a purgeable buffer station joined with and adjacent the substrate handling chamber, the purgeable buffer station configured for sealing and separately purging from the substrate handling chamber, the buffer station being located in position downstream of the front docking port.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Rejection of Claims 1-9

Claims 1-9 have been rejected under 35 U.S.C. §102(e) as being anticipated by Matsunaga et al. (2003/0053893).

Rejection of Claims 14-23

Claims 14-23 have been rejected under 35 U.S.C. §102(b) as being anticipated by Yonemitsu et al., U.S. Patent No. 6,143,083.

Rejection of Claims 10-18

Claims 10-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Matsunaga et al. in view of Ozawa et al., U.S. Patent No. 5,810,538.

VII. ARGUMENT

A. Rejection of Claims 1-9

In the Final Office Action, the Examiner finally rejected Claims 1-9 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 2003/0053893 to Matsunaga et al. (hereinafter "Matsunaga"). The Examiner argues that Matsunaga discloses all of the features of independent Claim 1.

Anticipation under 35 U.S.C. §102 requires the disclosure in a single piece of prior art of each and every feature of a claimed invention. *See Apple Computer, Inc. v. Articulate Systems, Inc.*, 234 F.3d 14, 57 USPQ2d 1057 (Fed. Cir. 2000). In order to anticipate, "every element and limitation of the claimed invention must be found in a single prior art reference, arranged as in the claim." *Brown v. 3M*, 265 F.3d 1349, 60 USPQ2d 1375 (Fed. Cir. 2001); see also *in re*

Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Thus, to anticipate, Matsunaga must disclose each and every feature of Claim 1 by disclosing the identical structure, arranged as recited in the claim. Claim 1 recites:

> 1. A semiconductor processing tool comprising:
>
> a first substrate handling chamber;
>
> a front docking port located on an outside surface of the first substrate handling chamber;
>
> a robot arm located in the first substrate handling chamber;
>
> a loadlock chamber joined to the first substrate handling chamber; and
>
> a buffer station adjacent the first substrate handling chamber and separate from the loadlock chamber, the buffer station being purged with an inert internal environment separate from the first substrate handling chamber, the buffer station having a rack defining multiple shelves for holding substrates.

Matsunaga discloses, as shown in Figure 1 and 5, a substrate processing apparatus including three processing units 61-63 positioned around and adjacent to a negative pressure wafer transfer chamber 11 having a wafer transfer device 10 (*i.e.*, robot). A loading chamber 20 and an unloading chamber 30 are also connected adjacently to the wafer transfer chamber 11 on one end and to a positive pressure wafer transfer chamber 40 on another end. The positive pressure wafer transfer chamber 40 has a wafer transfer device 42 therein, and a pod opener 50 provided at the wafer loading/unloading opening 49 for loading/unloading a pod P (FOUP) from a loading stage 51. The embodiment shown in Figure 5 also includes a buffer chamber 101 positioned around a negative pressure wafer transfer chamber 11.

With reference to Figure 5 of Matsunaga et al., the Examiner contends that "Matsunaga et al. disclose a first substrate handling chamber 12, front docking port 50, robot arm 10, rear substrate handling chamber 41, [and] buffer station 101 having a rack (Para. [0065]) configured to support a plurality of 300 mm silicon wafers." Final Office Action, page 2. As best understood, the Examiner appears to interpret Matsunaga's negative pressure wafer transfer chamber 11 as the claimed "first substrate handling chamber," Matsunaga's loading/unloading opening 49 as the claimed "front docking port located on an outside surface of the first substrate handling chamber," Matsunaga's wafer transfer device 10 as the claimed "robot arm located in

the first substrate handling chamber," Matsunaga's positive pressure wafer transfer chamber 40 as the claimed "loadlock chamber joined to the first substrate handling chamber," and Matsunaga's buffer chamber 101 as the claimed "buffer station adjacent the first substrate handling chamber and separate from the loadlock chamber."

Appellants respectfully submit that Matsunaga does not disclose each and every feature of Claim 1, and therefore does not anticipate Claims 1-9. If Matsunaga's chamber 11 (reference numeral 12 is the housing of chamber 11) serves as the recited first substrate handling chamber, then Matsunaga does not disclose or suggest a front docking port located on an outside surface of the first substrate handling chamber, as recited in Claim 1. As shown in Figures 1 and 5 of Matsunaga, the "loading/unloading opening" 49 and "loading stage" 51 are not on an outside surface of the chamber 11, but rather on an outside surface of chamber 40. On the other hand, if Matsunaga's chamber 40 is interpreted as the recited first substrate handling chamber (which does not appear to be the Examiner's position), then Matsunaga does not disclose or suggest a buffer station adjacent the first substrate handling chamber, as recited in Claim 1. As shown in Figure 5 of Matsunaga, the buffer chamber 101 is not adjacent to chamber 40 (which has a loading/unloading opening 49 and loading stage 51 located on an outside surface), but rather is adjacent to chamber 11, which does not have a front docking port located on an outside surface, as claimed. Thus, Matsunaga does not disclose or suggest a front docking port located on an outside surface of a substrate handling chamber and a buffer station adjacent the substrate handling chamber, as recited in Claim 1.

For the reasons discussed above, independent Claim 1 is allowable over Matsunaga. Claims 2-9, which depend from and include all of the limitations of Claim 1, are also patentable over Matsunaga. Furthermore, each of the dependent claims recites an additional novel and nonobvious combination of features of particular utility.

B. Rejection of Claims 14-23

In the Final Office Action, the Examiner finally rejected Claims 14-23 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,143,083 to Yonemitsu et al. (hereinafter "Yonemitsu"). The Examiner argued that Yonemitsu discloses all of the features of independent Claim 14. Independent Claim 14 recites:

14. A semiconductor processing tool comprising:

a substrate handling chamber;

a front docking port located on an outside surface of the substrate handling chamber, the port being capable of mating with a cassette;

a cassette rack internal to the docked cassette;

a purgeable buffer station joined with and adjacent the substrate handling chamber, the purgeable buffer station configured for sealing and separately purging from the substrate handling chamber, the buffer station being located in position downstream of the front docking port; and

a buffer station rack within the buffer station being configured to have multiple slots for holding substrates.

Yonemitsu discloses, in Figures 3 and 4, a semiconductor wafer processing apparatus 1 comprising a processing section 700, a transfer section 500, and a front section 100. The front section 100 comprises a plurality of load-lock modules 300, a wafer transfer device 20, and a cassette IN/OUT opening 13 for loading/unloading cassettes 10 into/out of an atmospheric pressure section 200. Each load-lock module 300 comprises an intermediate wafer holding chamber 30, a gate valve 92, and a front door valve 91. The intermediate wafer holding chamber 30 has a wafer holder 40 therein. As shown in Figure 5, the wafer holder 40 includes grooves 45 for holding a plurality of wafers. The transfer section 500 comprises a wafer transfer chamber 50 and a wafer-transfer vacuum robot 60 having (as shown in Figures 6A and 6B) arms 63, 65, 67 and rotational axles 62, 64, 66. The processing section 700 comprises a plurality of reaction chambers 70. As shown in Figure 4, the transfer section 500 is positioned between the processing section 700 and the front section 100.

With reference to Figure 4, the Examiner contends that "Yonemitsu et al. disclose a first substrate handling chamber 100, 500, front docking port 13, 200, robot arm 66, 20, and a buffer station having a rack 40." Final Office Action, page 4. The Examiner notes that "claim 14 does not recite a load lock chamber much less a load lock chamber separate from a buffer station," and that "Yonemitsu et al. certainly disclose a load lock that can function as a buffer station." Id. As best understood, the Examiner appears to interpret Yonemitsu's front section 100 and transfer section 500 together as the claimed "substrate handling chamber," Yonemitsu's cassette IN/OUT opening 13 as the claimed "front docking port located on an outside surface of the substrate handling chamber" (it is unclear how Yonemitsu's atmospheric pressure section 200 can be

interpreted as part of the claimed docking port), and one of Yonemitsu's load-lock modules 300 as the claimed "purgeable buffer station joined with and adjacent the substrate handling chamber."

Appellants respectfully submit that Yonemitsu does not disclose each and every feature of Claim 14, and therefore does not anticipate Claims 14-23. In particular, Yonemitsu does not disclose or suggest a purgeable buffer station. Skilled artisans will understand that a purgeable buffer station is one that is configured to receive a flow of a purge gas for expelling contaminants. For example, the present application discloses a buffer station having a purge valve and a gas inlet. Specification, para. [0036]; Fig. 1. In contrast, Yonemitsu discloses that the wafer holding chambers 30 of the load-lock modules 300 are adapted to be independently evacuated and depressurized. Yonemitsu, col. 2, lines 20-23; col. 3, lines 46-51; and col. 12, lines 7-9. Yonemitsu does not mention purging the chambers 30. In fact, Yonemitsu appears to teach away from purging by desiring a configuration in which "impurities are not outgassed" from the wafer holders 40 inside the wafer holding chambers 30. Id. at col. 5, lines 29-39; and col. 12, lines 37-41.

Yonemitsu also does not disclose a buffer station joined with and adjacent the substrate handling chamber, as claimed. As discussed above, the Examiner interprets Yonemitsu's front section 100 and wafer transfer section 500 together as the claimed first substrate handling chamber, and one of Yonemitsu's load-lock modules (containing an intermediate wafer holding chamber 30) as the claimed buffer station. However, Yonemitsu's load-lock module 300 is not joined with and adjacent the structure defined by the combination of the sections 100 and 500. Rather, as shown in Figure 4 of Yonemitsu, the load-lock module 300 is contained completely within (not adjacent to) said structure. The same is true even if Yonemitsu's front section 100 alone is interpreted as the claimed substrate handling chamber. In other words, the load lock module 300 is not joined with and adjacent the front section 100, but rather is within the front section 100. Further, Yonemitsu's wafer transfer section 500 alone cannot be interpreted as the claimed substrate handling chamber because the front port 13 is not located on an outside surface of the chamber 500 and the "atmospheric pressure section 200" is not a front docking port capable of mating with a cassette.

Claim 14 recites a number of interrelationships among the elements, and the Examiner may not apply one interpretation of the reference to meet one limitation and another interpretation of the reference to meet another limitation. Rather, one consistent interpretation of

the reference must simultaneously meet all of the claim limitations in order for the reference to anticipate. Thus, the Examiner cannot point to Yonemitsu's wafer transfer section 500 as the first substrate handling chamber to meet the recited limitation of a buffer station joined with and adjacent the first substrate handling chamber, while pointing to Yonemitsu's front section 100 as the first substrate handling chamber to meet the recited limitation of having a front docking port on the outside surface, the port being capable of mating with a cassette. For the reasons discussed above, Yonemitsu does not disclose a front docking port located on an outside surface of a substrate handling chamber and a purgeable buffer station joined with and adjacent the substrate handling chamber, as recited in independent Claim 14.

Independent Claim 14 is therefore allowable over Yonemitsu. Claims 15-23, which depend from and include all of the limitations of Claim 14, are also allowable over Yonemitsu. Furthermore, each of the dependent claims recites an additional combination of features of particular utility.

C. Rejection of Claims 10-18

Claims 10-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Matsunaga in view of U.S. Patent No. 5,810,538 to Ozawa et al. (hereinafter "Ozawa"). The Examiner has not established a *prima facie* case of obviousness because the art of record does not teach or suggest all of the claimed limitations of either independent Claim 10 or independent Claim 14. As discussed above with respect to Claim 1, Matsunaga does not disclose a front docking port located on an outside surface of a substrate handling chamber and a buffer station adjacent the substrate handling chamber. These limitations are also recited by independent Claims 10 and 14, which therefore recite limitations that are not disclosed or suggested by Matsunaga.

Ozawa discloses, in Figure 1, a piece of semiconductor manufacturing equipment comprising an enclosure 37 having a front shutter 38. A cassette stocker 24 is positioned for transferring, via the cassette transfer unit 40, cassettes 26 to/from the cassette stage 39, which is adjacent the front shutter 38. The tool also comprises a reaction chamber 15, a load-lock chamber 17, and a boat elevator 30 for loading and unloading a boat 18 to and from the reaction chamber 15. A carrying elevator 22 is face-to-face with the boat elevator 30. The carrying elevator 22 is provided with a wafer carrier 23 (for transferring as many wafers as desired from the boat elevator 18 to a cassette stocker 24), and a wafer holder (not shown) is designed such

that its pitch can be adjusted to match the difference in pitch of the wafer cassettes 26 or the boat 18. Ozawa, col. 4, lines 45-50.

Ozawa does not supply the deficiencies of Matsunaga. The Examiner has cited Ozawa solely for disclosing "a reduced pitch between a rack 18 and FOUP rack." Appellants respectfully submit that Ozawa does not disclose or suggest a front docking port located on an outside surface of a substrate handling chamber and a buffer station adjacent the substrate handling chamber. If Ozawa's front shutter 38 corresponds to the claimed "front docking port," then Ozawa's enclosure 37 would correspond to the claimed "substrate handling chamber," as recited in Claims 10 and 14. However, Ozawa does not teach or suggest any buffer station, much less a buffer station adjacent the enclosure 37.

In addition, it does not appear that Ozawa would have motivated a skilled artisan to modify Matsunaga to have a buffer station rack having a reduced pitch relative to FOUP shelves, as asserted by the Examiner. The Examiner contends that it would have been obvious to modify the Matsunaga apparatus to include a buffer station rack having a reduced pitch relative to FOUP shelves, because Ozawa teaches "to reduce boat cycle-through times" by allowing "multiple wafers from smaller cassettes to be placed in a single wafer boat allowing increase[sic] wafer production during one boat cycle-through." Final Office Action, page 5. However, nothing in Ozawa suggests or indicates that a reduced pitch buffer station rack would "reduce boat cycle-through times." Ozawa merely recognizes that wafer cassettes 26 and the internal boat 18 can have different pitches, and proposes a wafer holder with an adjustable pitch to match either the cassettes or the boat. Ozawa does not teach or suggest reducing "cycle-through times," much less reducing "cycle-through times" by using a reduced pitch buffer station rack. Ozawa therefore provides no motivation for modifying the Matsunaga apparatus (which does not even meet the other recited claim limitations) with a reduced pitch buffer station rack.

Thus, for the reasons discussed above, the asserted combination of Matsunaga and Ozawa does not meet the limitations of Claim 10 or 14, let alone the unique combinations of limitations of 11-13 and 15-18, which depend from and include all of the limitations of Claim 10 or 14. Also, as explained above, the skilled artisan would not have been motivated to combine Matsunaga and Ozawa in the manner asserted. Claims 10-18 are therefore allowable over Matsunaga and Ozawa, either alone or in combination.

D. Conclusion

In summary, Appellants submit that the claims that are subject to this appeal, Claims 1-18, are allowable over the art of record. To summarize, Appellants submit that Claims 1-23 are patentable over the art of record because none of the cited references, either alone or in combination, teaches or suggests a front docking port located on an outside surface of a substrate handling chamber and a buffer station adjacent the substrate handling chamber, which is recited in all of the pending claims. Also, there is no suggestion or motivation found in the prior art of record to modify one of the primary references (Matsunaga et al.) to include a buffer station rack having a reduced pitch relative to FOUP shelves.

VIII. CLAIMS APPENDIX

Attached hereto as the Claims Appendix is a copy of the finally rejected claims in the present case.

IX. EVIDENCE APPENDIX

Not applicable.

X. RELATED PROCEEDINGS APPENDIX

Not applicable.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: February 8, 2007

By: _____

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CLAIMS APPENDIX
(Claims as finally rejected)

1. A semiconductor processing tool comprising:

a first substrate handling chamber;

a front docking port located on an outside surface of the first substrate handling chamber;

a robot arm located in the first substrate handling chamber;

a loadlock chamber joined to the first substrate handling chamber; and

a buffer station adjacent the first substrate handling chamber and separate from the loadlock chamber, the buffer station being purged with an inert internal environment separate from the first substrate handling chamber, the buffer station having a rack defining multiple shelves for holding substrates.

2. The semiconductor processing tool according to Claim 1, wherein the rack is configured to support a plurality of 300 mm silicon wafers.

3. The semiconductor processing tool according to Claim 1, further comprising a rear substrate handling chamber, where the loadlock chamber is located between the first substrate handling chamber and the rear substrate handling chamber.

4. The semiconductor processing tool according to Claim 1, wherein the buffer station is further configured to create an inert environment which is selectively isolated from the first substrate handling chamber.

5. The semiconductor processing tool according to Claim 4, wherein the buffer station is further configured to be selectively purged.

6. The semiconductor processing tool according to Claim 4, wherein the buffer station rack is configured to allow the robot arm to be capable of accessing the entire buffer station rack through the use of a z-motion of the robot arm.

7. The semiconductor processing tool according to Claim 1, wherein the buffer station is configured to have a internal volume less than or equal to about 18.3 liters.

8. The semiconductor processing tool according to Claim 7, wherein the buffer station rack is configured to support twenty-five 300 mm silicon wafers.

9. The semiconductor processing tool according to Claim 1, wherein the loadlock chamber is configured to have an internal volume less than or equal to about 9.156 liters.

10. A semiconductor processing tool comprising:

a first substrate handling chamber;

a front docking port located on the outside surface of the first substrate handling chamber;

a robot arm located in the first substrate handling chamber;

a loadlock chamber joined to the first substrate handling chamber; and

a buffer station adjacent the first substrate handling chamber and separate from the loadlock chamber, the buffer station being purged with an inert internal environment separate from the first substrate handling chamber, the buffer station having a rack defining multiple shelves for holding substrates, wherein the shelves of the buffer station rack have a reduced pitch relative to shelves of a front opening unified pod (FOUP) for the same size substrates.

11. The semiconductor processing tool according to Claim 1, wherein the robot arm is configured to employ a variable pitch end effector having multiple end effector shelves.

12. The semiconductor processing tool according to Claim 1, wherein the first substrate handling chamber is configured to operate at atmospheric pressure.

13. The semiconductor processing tool according to Claim 1, wherein the first substrate handling chamber is configured to operate at reduced pressure.

14. A semiconductor processing tool comprising:

a substrate handling chamber;

a front docking port located on an outside surface of the substrate handling chamber, the port being capable of mating with a cassette;

a cassette rack internal to the docked cassette;

a purgeable buffer station joined with and adjacent the substrate handling chamber, the purgeable buffer station configured for sealing and separately purging from the substrate handling chamber, the buffer station being located in position downstream of the front docking port; and

a buffer station rack within the buffer station being configured to have multiple slots for holding substrates.

15. The semiconductor processing tool according to Claim 14, further comprising a loadlock chamber joined with the substrate handling chamber, the loadlock chamber having a

loadlock rack with a substrate capacity of less than one third of a substrate capacity of the cassette.

16. The semiconductor processing tool according to Claim 15, further comprising a rear substrate handling chamber where the loadlock chamber is located between the substrate handling chamber and the rear substrate handling chamber.

17. The semiconductor processing tool according to Claim 15, wherein the substrate capacity of the loadlock chamber is 1 to 7 substrates.

18. The semiconductor processing tool according to Claim 15, wherein the loadlock rack is configured to support a plurality of 300 mm silicon wafers.

19. The semiconductor processing tool according to Claim 14, wherein the substrate handling chamber is configured to operate at standard atmospheric pressure.

20. The semiconductor processing tool according to Claim 14, wherein the substrate handling chamber is configured to operate at reduced pressure.

21. The semiconductor processing tool according to Claim 14, wherein the buffer station rack has a reduced relative spacing between the rack slots as compared with a relative spacing between slots of the cassette.

22. The semiconductor processing tool according to Claim 14, wherein the buffer station rack is a reduced pitch rack configured to allow a robot arm to be capable of accessing the entire buffer station rack through the use of a robot arm's z-motion.

23. The semiconductor processing tool according to Claim 14, further comprising a robot arm configured to have a variable pitch end effector designed to transfer multiple substrates from the cassette rack to the buffer station rack, the cassette rack having unequal slot pitch relative to the buffer station rack.

EVIDENCE APPENDIX

Not applicable.

RELATED PROCEEDINGS APPENDIX

Not applicable.

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